FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 500797.02 (30005/US/2)	APPLICATION NO. Not Yet Assigned
INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANTS Brian Johnson and Ronnie M. Harrison	
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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
GJP	IW	0 655 741 A2	5/31/95	EP			X	
	IX	0 655 834 A1	5/31/95	EP			X	
	IY	WO 95/22200	8/17/95	PCT			X	
	IZ	WO 95/22206	8/17/95	PCT			X	
	JA	0 680 049 A2	11/2/95	EP			X	
	JB	0-7319577	12/8/95	JP (+ Abstract)			X	
	JC	0 703 663 A1	3/27/96	EP			X	
	JD	0 704 848 A3	4/3/96	EP			X	
	JE	0 704 975 A1	4/3/96	EP			X	
	JF	WO 96/10866	4/11/96	PCT			X	
	JG	0 767 538 A1	4/9/97	EP			X	
	JH	WO 97/14289	4/24/97	PCT			X	
GJP	JI	WO 97/42557	11/13/97	PCT			X	

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

GJP	JJ	Alvarez, J. et al. "A Wide-Bandwidth Low Voltage PLL for PowerPC ™ Microprocessors" IEEE IEICE Trans. Electron., Vol. E-78. No. 6, June 1995, pp. 631-639
	JK	Anonymous, "400MHz SLDRAM, 4M X 16 SLDRAM Pipelined, Eight Bank, 2.5 V Operation," SLDRAM Consortium Advance Sheet, published throughout the United States, pp.1-22
	JL	Anonymous, "Draft Standard for a High-Speed Memory Interface (SyncLink)", Microprocessor and Microcomputer Standards Subcommittee of the IEEE Computer Society, Copyright 1996 by the Institute of Electrical and Electronics Engineers, Inc., New York, NY, pp. 1-56
	JM	Anonymous, "Programmable Pulse Generator", IBM Technical Disclosure Bulletin, Vol. 17, No. 12, May 1975, pp. 3553-3554
GJP	JN	Arai, Y. et al., "A Time Digitizer CMOS Gate-Array with a 250 ps Time Resolution", XP 000597207, IEEE Journal of Solid-State Circuits, Vol. 31, No.2, February 1996, pp. 212-220

EXAMINER	GARY J. PORTKA	DATE CONSIDERED	9/6/06

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

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		OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)
GJP	JO	Anonymous, "Pulse Combining Network", IBM Technical Disclosure Bulletin, Vol. 32, No. 12, May 1990, pp. 149-151
	JP	Anonymous, "Variable Delay Digital Circuit", IBM Technical Disclosure Bulletin, Vol. 35, No. 4A, September 1992, pp. 365-366
	JQ	Arai, Y. et al., "A CMOS Four Channel x 1K Time Memory LSI with 1-ns/b Resolution", IEEE Journal of Solid-State Circuits, Vol. 27, No. 3, M, 8107 March, 1992, No. 3, New York, US, pp. 359-364 and pp. 528-531
	JR	Aviram, A. et al., "OBTAINING HIGH SPEED PRINTING ON THERMAL SENSITIVE SPECIAL PAPER WITH A RESISTIVE RIBBON PRINT HEAD", IBM Technical Disclosure Bulletin, Vol. 27, No. 5, October 1984, pp. 3059-3060
	JS	Bazes, M., "Two Novel Fully Complementary Self-Biased CMOS Differential Amplifiers", IEEE Journal of Solid-State Circuits, Vol. 26, No. 2, February 1991, pp. 165-168
	JT	Chapman, J. et al., "A Low-Cost High-Performance CMOS Timing Vernier for ATE", IEEE International Test Conference, Paper 21.2, 1995, pp. 459-468
	JU	Cho, J. "Digitally-Controlled PLL with Pulse Width Detection Mechanism for Error Correction", ISSCC 1997, Paper No. SA 20.3, pp. 334-335
	JV	Christiansen, J., "An Integrated High Resolution CMOS Timing Generator Based on an Array of Delay Locked Loops", IEEE Journal of Solid-State Circuits, Vol. 31, No. 7, July 1996, pp. 952-957
	JW	Combes, M. et al., "A Portable Clock Multiplier Generator Using Digital CMOS Standard Cells", IEEE Journal of Solid-State Circuits, Vol. 31, No. 7, July 1996, pp. 958-965
	JX	Donnelly, K. et al., "A 660 MB/s Interface Megacell Portable Circuit in 0.3 μm-0.7 μm CMOS ASIC", IEEE Journal of Solid-State Circuits, Vol. 31, No. 12, December 1996, pp. 1995-2001
	JY	Goto, J. et al., "A PLL-Based Programmable Clock Generator with 50- to 350-MHz Oscillating Range for Video Signal Processors", IEICE Trans. Electron., Vol. E77-C, No. 12, December 1994, pp. 1951-1956
	JZ	Gustavsion, David B., et al., "IEEE Standard for Scalable Coherent Interface (SCI)," IEEE Computer Society, IEEE Std. 1596-1992, August 2, 1993.
	KA	Hamamoto, T., "400-MHz Random Column Operating SDRAM Techniques with Self-Skew Compensation", IEEE Journal of Solid-State Circuits, Vol. 33, No. 5, May 1998, pp. 770-778
GJP	KB	Ishibashi, A. et al., "High-Speed Clock Distribution Architecture Employing PLL for 0.6μm CMOS SOG", IEEE Custom Integrated Circuits Conference, 1992, pp. 27.6.1-27.6.4

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